Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A computer system, comprising:

a first processor;

a second processor for use as a coprocessor to the first processor;

a coprocessor controller;

a memory;

a buffer memory from which the second processor loads data and to which the second processor stores data, wherein the buffer memory is adapted to load data from the memory and store data to the memory; ~~and~~

a first decoupling element; and

a second decoupling element,

wherein computations are passed to the second processor from the first processor through the first decoupling element, such that the second processor executes computations passed from the first processor through the first decoupling element, and wherein the second processor receives data from and writes data to the memory, and wherein the coprocessor controller controls the activity of the second processor to ensure execution of the second processor is correctly ordered with respect to loads from memory, whereby the execution of computations by the second processor is decoupled from the operation of the first processor such that the second processor executes computations passed from the first processor through the first decoupling element while the first processor is providing further instructions to the first decoupling element, and further wherein memory instructions relating to movement of data between the buffer memory and the memory are passed to the buffer memory from the first processor through the second decoupling element, such that the buffer memory consumes instructions derived from the first processor through the second decoupling element, whereby the processing of memory instructions by the buffer memory is decoupled from the operation of the first processor.

2. (currently amended) A computer system as claimed in claim 1, wherein the first decoupling element is a coprocessor instruction queue, wherein computations are added to the coprocessor instruction queue by the first processor and consumed from the coprocessor instruction queue by the coprocessor.

3. (currently amended) A computer system as claimed in claim 1, wherein the first decoupling element is a state machine, wherein information to provide computations to the second processor is provided to the state machine by the first processor, and computations are provided in an ordered sequence to the second processor by the state machine.

4. (currently amended) A computer system as claimed in claim 1, wherein the first decoupling element is a third processor, wherein information to provide computations to the second processor is provided to the third processor by the first processor, and computations are provided in an ordered sequence to the second processor by the third processor.

5. (previously presented) A computer system as claimed in claim 1, wherein the second processor is configurable.

6. (original) A computer system as claimed in claim 5, wherein the second processor is adapted to be configured in accordance with a configuration downloaded from the memory.

7. (previously presented) A computer system as claimed in claim 1, wherein the first processor is able to switch tasks during execution of computations by the second processor.

8. (canceled)

9. (currently amended) A computer system as claimed in claim [[8]] 1, wherein the memory is dynamic random access memory, and the buffer memory is adapted to load data from, or store data to, the buffer memory in bursts.

10. (canceled)

11. (currently amended) A computer system as claimed in claim ~~10~~ 1, wherein the second decoupling element is a buffer memory instruction queue, wherein memory instructions are added to the buffer memory instruction queue by the first processor and consumed from the buffer memory instruction queue by the buffer memory.

12. (original) A computer system as claimed in claim 11, wherein the second decoupling element is a state machine, wherein information to provide memory instructions to the buffer memory is provided to the state machine by the first processor, and memory instructions are provided in an ordered sequence to the buffer memory by the state machine.

13. (currently amended) A computer system as claimed in claim ~~10~~ 1, wherein the second decoupling element is a fourth processor, wherein information to provide memory instructions to the buffer memory is provided to the fourth processor by the first processor, and memory instructions are provided in an ordered sequence to the buffer memory by the fourth processor.

14. (currently amended) A computer system as claimed in claim [[8]] 1, further comprising a synchronisation mechanism to synchronise transfer of data between the buffer memory and the memory with execution of computations by the second processor.

15. (previously presented) A computer system as claimed in claim 14, wherein the synchronisation mechanism is adapted to block execution of computations by the second processor on data which has not yet been loaded to the buffer memory from

the memory, and is adapted to block execution of memory instructions for storage of data from the buffer memory to the memory where relevant computations have not yet been executed by the second processor.

16. (previously presented) A computer system as claimed in claim 15, adapted such that when execution of computations or memory instructions is blocked by the synchronisation mechanism, other computations or memory instructions which are not blocked by the synchronisation mechanism may be executed.

17. (previously presented) A computer system as claimed in claim 1, wherein the first processor is the central processing unit of a computer device.

18. (canceled)